WHAT IS CLAIMED IS:

1. A standardized silicon platform chip, comprising:

a substrate having a substrate surface that includes an array of unconnected transistors that surround a plurality of islands; the plurality of islands including circuit elements that are interconnectable within each island to form a plurality of varied circuit functions for each of the islands; the varied circuit functions including both application functions and clock functions;

a plurality of interconnect layers deposited over the substrate surface, the interconnect layers interconnecting the circuit elements within each island to complete the plurality of varied circuit functions; and

the varied circuit functions including varied levels of integration including at least gates, flip-flops, clock trees, and oscillators that are custom connectable to the array of unconnected transistors to form standard clock resources for the standardized silicon platform integrated circuit.

2. The standardized silicon platform chip of Claim 1 wherein the application functions are selected to fill needs in a selected application niche.

3. The standardized silicon platform chip of Claim 1 wherein at least some of the varied circuit functions are connectable as both clock functions and application functions.

4. The standardized silicon platform chip of Claim 1 wherein the clock functions are connectable to form multiphase clock generators.

5. The standardized silicon platform chip of Claim 4 wherein the multiphase clock generators are connectable to generate a plurality of synchronous clock outputs.

6. The standardized silicon platform chip of Claim 5 wherein the synchronous clock outputs have a closed timing specification.

7. The standardized silicon platform chip of Claim 1 wherein the array of unconnected transistors comprise N channel field effect transistors.

8. The standardized silicon platform chip of Claim 1 wherein the array of unconnected transistors comprise P channel field effect transistors.

9. A standardized silicon platform chip including the standardized silicon platform chip of Claim 1 and further comprising:

a second plurality of interconnects deposited over the substrate surface and selectively interconnecting a selected subset of the islands with selected subset of the array of unconnected transistors to complete a selected customized clock function.

10. The standardized silicon platform chip of Claim 9 wherein the second plurality of interconnects also complete a selected application function supported by the selected clock function.

11. The standardized silicon platform chip of Claim 10 wherein the selected application function is in a selected application niche.

12. The standardized silicon platform chip of Claim 9 wherein the second plurality of interconnects connects the clock resource to form a multiphase clock generator.

13. The standardized silicon platform chip of Claim 12 wherein the multiphase clock generator generates a plurality of synchronous clock outputs.

14. The standardized silicon platform chip of Claim 13 wherein the synchronous clock outputs have a closed timing specification.

15. A computer-readable medium having computer-executable instructions for performing a custom interconnect design for a standardized silicon platform chip, comprising:

standard clock resource data stored on the computer-readable medium;

physical layout data stored on the computer-readable medium;

instructions for prompting custom clock requirements from a user and for storing the custom clock requirements on the computer readable medium;

a composing program for composing a clock circuit for the standardized silicon platform chip and providing a clock design output;

a resource selector program for selectively applying the standard clock resource data, the physical layout data and custom clock requirements to the composing program;

a view generator program that generates a plurality of views of the clock design output;

a user interaction program that displays problems with the views of the clock design output and potential solutions to the problems to the user for selection and implementation to provide a closed design; and

a design qualify program that tests the closed design for errors and stores the closed design on the computer-readable medium if it is free of errors.

16. The computer-readable medium of Claim 15, further comprising:

an ad-hoc clock detector program that interacts with the composing program to identify instances of ad-hoc clocking circuitry in the custom silicon platform chip design.

17. The computer-readable medium of Claim 15, further comprising:

a clock compiler program interacting with the composing program to provide compiled clock designs to the composing programs.

18. The computer-readable medium of Claim 15, wherein the closed design is applied to a standardized silicon platform chip that includes islands with interconnections that provide varied circuit functions

surrounded by an array of unconnected transistors, and the closed design applies second interconnections that connect selected islands to selected unconnected transistors to customize the standardized silicon platform chip.